Liquid Crystal on VLSI Silicon Optical Phased Array

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ABSTRACT

Several applications for solid-state, random access beam directors have emerged in recent years, including scanners, laser radar components, interconnects, elements for addressing holographic storage, beam routing devices, and adaptive switching networks. We discuss implementation of optical phased arrays using a liquid crystal on silicon approach. By using very large scale integration (VLSI) technology, each element of the array is individually addressable. This allows the device to spatially correct both static and dynamic phase distortions as it steers the beam (or field of regard). In addition, this technology lends itself to the possibility of scaling to large (several centimeters) aperture.

Currently VLSI foundries are pushing for small feature size and higher operating voltages. These ongoing developments in integrated circuit fabrication processes result in devices exhibiting excellent electrical performance, but poor optical quality. Increased reflectivity and planarization are necessary to produce high efficiency beam steering devices. Steps taken to improve optical performance of silicon backplanes will also be discussed.

Keywords: beam steering, liquid crystal on silicon, optical phased array

1. INTRODUCTION

Diffractive beamsteerers are essentially an optical phased array analogous to some radar systems. Alternatively, the optical phased array can be thought of as a quantized multiple level phase grating. The more phase levels used in the array, the higher the diffraction efficiency. For example, a binary phase grating ideally provides a diffraction efficiency of 40.5% in each of the two first order diffracted beams. If more than two phase levels are used, and the complex plane is uniformly sampled, the profile becomes asymmetric like a blazed grating which results in an increase in the efficiency of the favored first diffracted order. For a quantized phase grating using three phase levels the ideal first order diffraction efficiency is 68.4%, while for 4 phase levels, it increases to 81%. For more than four levels the improvement in diffraction efficiency with increasing number of phase levels slows. At 5 levels the percentage of light diffracted into the first order is ideally 87.5% and for 8 phase levels the ideal first order diffraction efficiency is 94.9%.

Optical phased arrays can be implemented using liquid crystals to produce the phase shift. Liquid crystal optical modulators offer several advantages including large modulation depth, inertialess switching, low power dissipation, potential for large aperture operation, and low cost. Liquid crystal modulators can also provide for a variety of optical transmittance characteristics. The different types of modulation that can be achieved with liquid crystal devices include: bipolar, real-axis, phase-only, coupled phase-amplitude and broad band phase shifters[1]. The various optical transmittance characteristics of liquid crystal modulators depend on the modulator architecture and the material used, as does the response time. Response times can range from several ms to 1 μs.

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Due to the effects of fringing fields on the liquid crystal between electrode lines, the actual phase profile is not a series of quantized steps but is smoothed such that the device more closely resembles a blazed grating. Ideal blaze gratings approach a diffraction efficiency of 1. In addition to the phase profile, device efficiency also depends on the effective fill factor. The effective fill factor is governed by the size of the flyback region (where the phase reset defining a grating period occurs) relative to the size of the grating period[2]. That is, the far field diffraction pattern is convolved with a pixel function which envelopes the far field such that efficiency decreases for larger angles. In addition to non-ideal phase profiles, there is an insertion loss that needs to be considered[3]. The insertion loss includes such things as non-ideal mirror reflectivity, Fresnel losses, absorption by and scatter due to the modulating medium and/or structure.

The deflection angle for a diffractive beamsteerer, θ_m, is given by

$$\theta_m = \sin^{-1}\left(\frac{m\lambda}{d}\right) \quad . \qquad (1)$$

Here m is the diffracted order (usually only the first order is considered), λ is the vacuum wavelength and d is the (variable) grating period. Note that due to the nature of diffractive devices, steering is in general not continuous, though techniques can be used to make the steering appear continuous. A major advantage of diffractive devices is that the addressable angles can be randomly accessed.

An additional advantage of diffractive beamsteerers is the potential for two-dimensional steering using a single device. However, fabrication limitations restrict two-dimensional steering to small angles at this time. One-dimensional diffractive beamsteerers can be cascaded to steer in two dimensions.

2. PROTOTYPE LIQUID CRYSTAL OPTICAL PHASED ARRAY

2.1 VLSI Backplane Specifications

The prototype backplane has been fabricated and has the following specifications:

- The electrode elements are 0.9 micron wide lines separated by 0.9 micron wide spaces.
- There are 4096 individually addressable electrodes.
- The number of resolvable spots will be more than 128[4].
- The aperture is designed to be 7.4 mm square. In the future (2-3 years), we intend to increase this size.
- The individual pixels are 0.9 microns wide and 7.4 mm long.
- Our design wavelength is 1.5 μm. However, these devices will be adaptable to other wavelengths, within the basic constraints of the backplane and liquid crystal material.

The second generation backplane that we are currently developing is similar, but the wafers are being planarized at the VLSI foundry. The primary change in the VLSI design between the prototype and the latest backplane is the duty cycle of the pixels. The pixels are 1.0 micron wide and the interpixel gap is 0.8 microns for the updated design.

2.2 LC Materials

The VLSI backplane is limited to a maximum of 5V of output. While 40 V levels are possible for VLSI devices, the high voltage technology is not yet available for the 0.6 micron process which is being used to obtain the sub-micron interpixel gap. Moreover, the industry is being driven toward higher resolution lithography which can be obtained more easily with lower driving voltages. Consequently, it is necessary that the LC used for the modulator provide a full wave of modulation depth at signals of 5 Volts or less. The voltage responses of some of the potential LC candidates have been measured. Percentage of the desired modulation depth as a function of driving voltage has been measured for the commercial LC materials: E7, E44, and BL066 all from Merck. Each of the three cells was gapped to a thickness that corresponds to a half-wave of retardation at 1500 nm. The modulators are intended to provide information applicable to the reflection mode configuration of the beamsteerer. Figure 1 is a plot showing the modulation vs. voltage for each of the three commercial candidates. BL066 is a low threshold mixture and exhibits the largest modulation depth for voltages less than 5V. Using the exact half-wave gap thickness, none of these materials provides sufficient modulation depth at likely addressing levels. That is, complete switching to obtain homeotropic director orientation requires more than 5 V. One possible solution would be to use a much thicker gap; however, speed and diffraction effects become issues. A better approach involves doping the LC materials with dye to enhance the dielectric anisotropy and improve the switching characteristics for TTL level voltages.

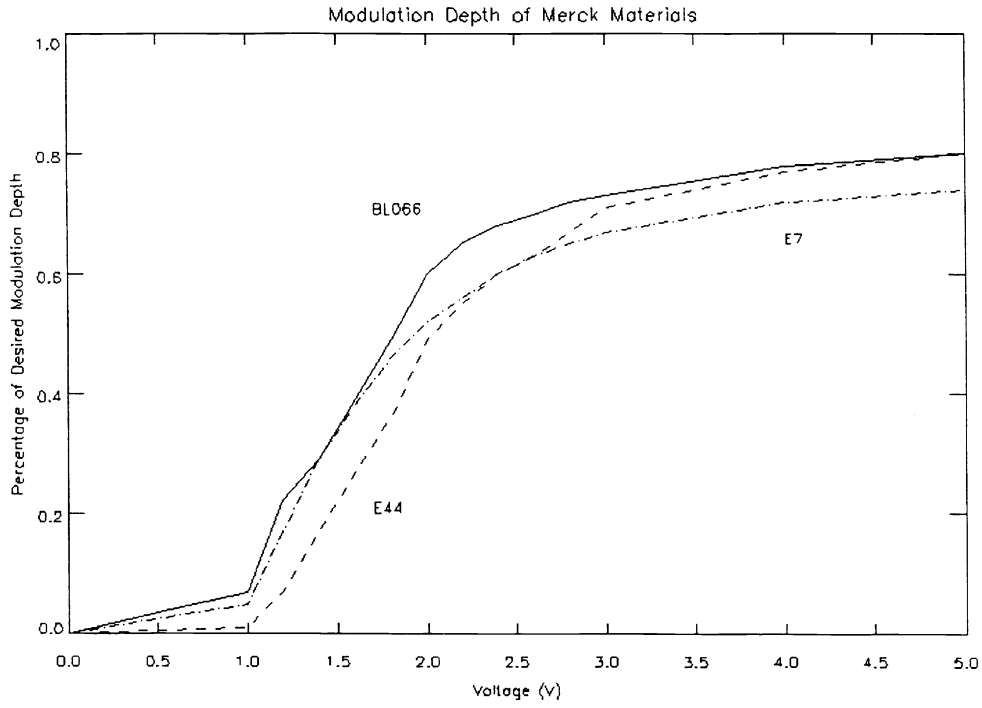

Figure 1. Percent modulation depth as a function of voltage. The desired modulation depth is half-wave at 1500 nm. Thus, these devices mimic a reflection mode modulator. Physical device thicknesses were 4 microns for the BL066 and E7 and 3.5 microns for the E44.

We have used the azo-dye designated C5 to enhance the dielectric anisotropy of two liquid crystal materials[5]. The dye also slightly enhances the optical anisotropy of the materials so thinner cells can be used to achieve the desired modulation depth. Figure 2 is a plot of the percentage of modulation depth for

BL066 and PTTP, a high birefringent experimental material[6]. We also investigated modulators using these materials after they had been doped with the azo-dye. Note that the threshold voltage and saturation voltage decreases for both of these materials when doped with the azo-dye. We achieved good miscibility for 20% dye in the Merck material, and 10% dye in the PTTP. The amount of dye in each material could probably be increased by half again as much, but doubling the content might be pushing the limitations of the dye solubility in the respective materials. These are encouraging results, especially for the dye-doped BL066 which achieved full modulation at an rms voltage level below 1.5 V for the device measured here. For this material, TTL level voltages, even addressed through a dielectric stack, will attain the desired modulation depth. More will be known once the backplanes described in the following section have been thoroughly tested.

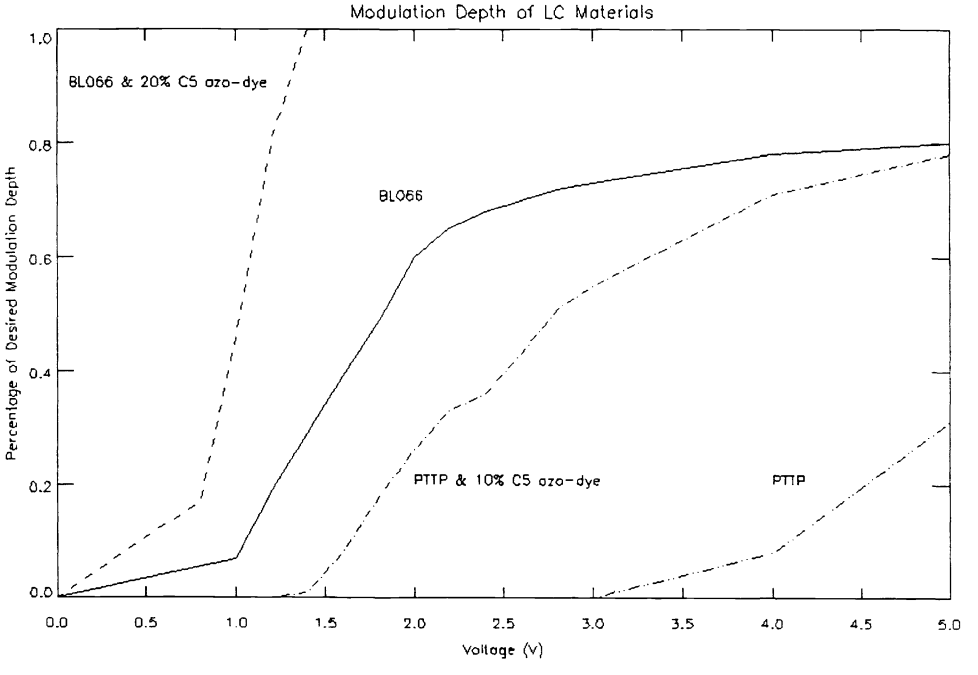

Figure 2. Modulation Depth as a function of applied Voltage (rms) for two different liquid crystal materials and their dye-doped counterparts.

3. DIFFRACTION EXPERIMENTS

3.1 VLSI backplane diffraction

The prototype backplanes have been tested optically. The initial characterization concentrated on the innate diffraction properties of the backplanes. The optical set-up for the test is shown in Figure 3. Light from a laser is polarized and directed onto the backplane. The reflected light is analyzed and detected. The lower orders of the diffraction pattern, corresponding to the data presented below in this section are shown in Figure 4.

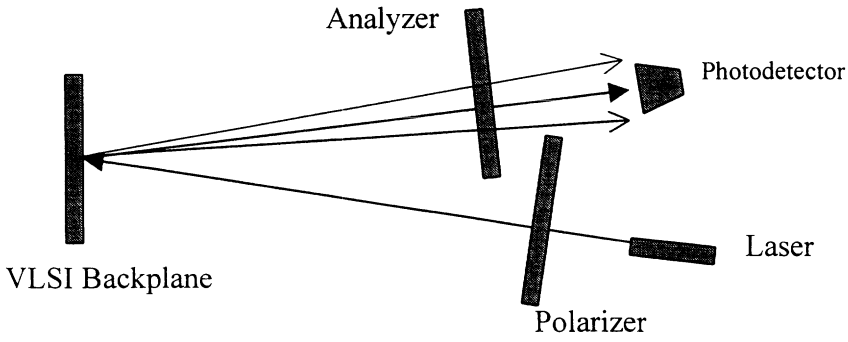

Figure 3. VLSI backplane diffraction test set–up.

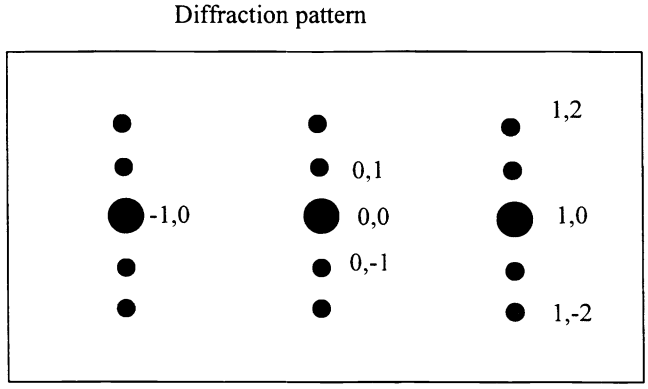

Figure 4. Typical diffraction pattern for the VLSI backplanes. The horizontal orders are due to the electrodes, while the vertical orders are due to the slotted ground planes.

For the first set of diffraction experiments a bare backplane is illuminated. Initially the source is a helium neon laser operating at 632.8 nm. The list below gives the normalized intensity in some of the lower orders depicted in Figure 4. Note that about 22.5% remains in the zero order. This is an improvement by a factor of 2 over our current 2-D SLM devices and an indication of the reduced surface roughness of the Metal 2 electrodes.

The results presented here are for the incident light polarized parallel to the electrodes. Similar diffraction intensities were obtained for light polarized perpendicular to the electrodes. This is an interesting result in that a high frequency grating should be strongly polarization dependent. One possibility for the similarity of the diffraction characteristics could be that polarization effects are negated by the indiscriminant absorption of approximately 50% of the light by the AR coating that was previously deposited during VLSI lithographic processing. Removal of this coating has become a key task for the second-generation backplane currently under development.

Results of HeNe probe $\lambda = 632.8\ nm$ incident on a bare backplane:

$I_{inc}=1$ $I_{0,0}=0.225$

$I_{1,0}=0.081$ $I_{1,-1}=7.4\cdot10^{-4}$

$I_{1,-2}=6.6\cdot10^{-4}$ $I_{-1,0}=0.069$

$I_{-1,-2}=7.6\cdot10^{-4}$ $I_{2,0}=0.048$

$I_{2,-1}=9.5\cdot10^{-4}$ $I_{-2,0}=0.052$.

Next, the laser source was changed to a diode laser operating at 1540 nm. The results for the dominant lower orders are presented below. Again, for the results shown here, the incident light is polarized coincident with the direction of the electrode array. Similar intensities were obtained for the orthogonal polarization. For this wavelength even more of the incident light remains in the zero order. This can be attributed to the relative size of the two test wavelengths with respect to the electrode period.

Diode laser $\lambda = 1540\ nm$ incident on a bare backplane:

$I_{inc}=1$ $I_{0,0}=0.621$

$I_{1,0}=0.027$ $I_{-1,0}=0.016$.

3.2 Liquid crystal beamsteerer preliminary results

For the second set of experiments a backplane that has been gapped and filled with nematic liquid crystal is probed. The liquid crystal used, RDK-01160, is a mixture from RODIC Ltd. and exhibits a birefringence of 0.2 in the visible. The beamsteerer is not electrically addressed for this set of experiments. Different devices exhibit different visual optical quality, for example random stripes coincident with the gap between electrodes occur. In some devices there are only a few of these stripes, while in others the number of defects can be significant. We believe these stripes are an artifact of the filling process. For the filled devices, the diffraction efficiencies depend on the quality of the optical head. The stripes along the electrodes can increase scattering into higher orders (from 0^{th} order) by a factor of two. The results presented below are for the best (fewest stripes) device to date.

For this series of experiments the set-up is again the same as depicted in Figure 3. The diffraction efficiencies for the diode laser $\lambda = 1540\ nm$ incident are:

$I_{inc}=1$, $I_{0,0}=0.448$, and, $I_{-1,0}=6.3\cdot10^{-4}$.

The decrease in the zero order diffraction intensity is probably due to scattering losses and index mismatch. The intensities were similar for both polarizations.

An electrically addressed device has been examined under a microscope. Figure 5 is a photograph of a wedge pattern written to the device. The gray scale represents a phase difference. Figure 6 is a magnified view of the beamsteerer with a voltage ramp applied.

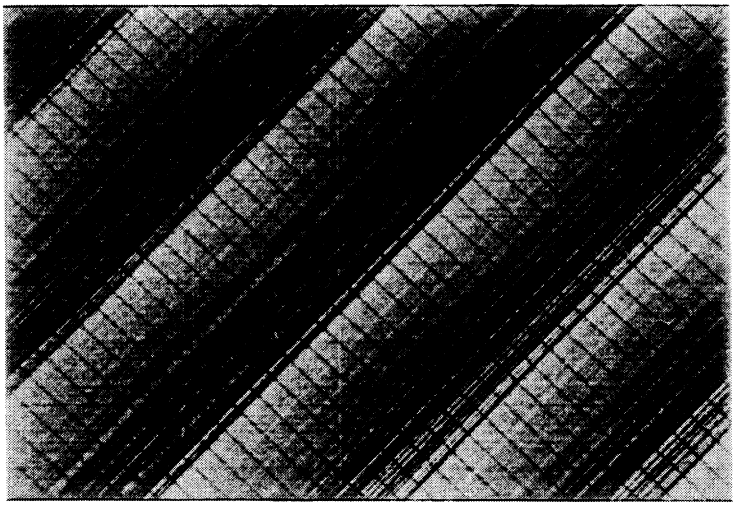

Figure 5. Prototype liquid crystal beamsteerer with a repeating voltage ramp applied every 128 electrodes. The slotted ground planes underneath and orthogonal to the stripes are approximately 30 microns wide.

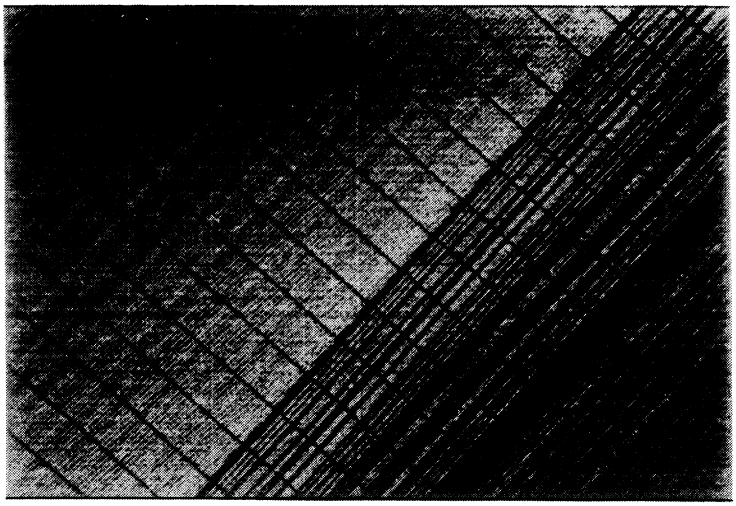

Figure 6. Close-up photograph of prototype nematic liquid crystal beamsteerer with an applied voltage ramp. The individual pixel pitch of 1.8 μm is resolvable at this magnification.

After a series of experiments on devices fabricated using the prototype die, we have determined that a six micron thick liquid crystal layer of BL066 from Merck has a modulation depth of at least 1 wave at 1550 nm for an applied voltage up to 5 V rms. For this demonstration, the increased thickness allows full modulation without completely switching the LC into the homeotropic director orientation, and without doping the LC with a die to enhance the dielectric anisotropy. Due to unfavorable diffraction effects and reduced speed for thicker devices, more testing with dye-doped materials is scheduled. Figure 7

demonstrates that the intensity cycles through at least one period (or 1 wave of retardation) for linearly polarized laser light at 1550 nm.

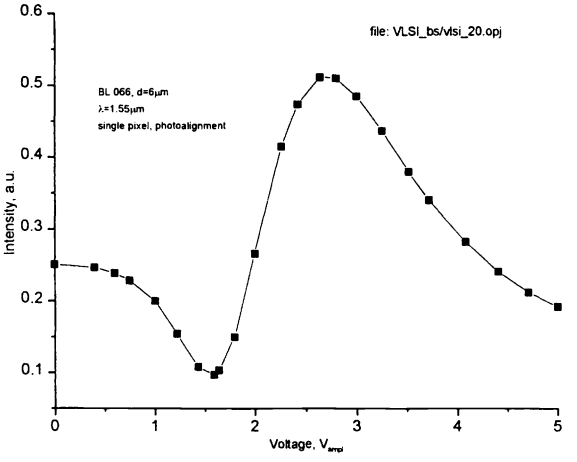

Figure 7. Intensity as a function of voltage, for linearly polarized light incident on a prototype backplane filled with BL066.

For the device which produced the results shown in Figure 7 the alignment was buffed polyimide on the cover glass and photo-aligned polymide on the backplane. This device reflected 54%-58% of the incident light into the zero order. A coating or alignment layer on the backplane appears to be critical. Devices that had alignment only on the cover glass exhibited defect stripes and reflected only 30%-43% of the incident light into the zero order.

A dielectric stack has been deposited on five of the prototype die. The mirror design is a five-layer, (three high index, two low index) quarter-wave stack. The mirror thickness is 1.04 microns. This dielectric layer is in addition to the two-micron thick conformal SiOx coating that the prototype die is passivated with. While a witness sample of the dielectric stack on a glass substrate exhibited 75% reflection at a wavelength of 1550 nm, the backplanes are diffractive because they have not been planarized and the amount of light reflected to the zero order ranges from 47% to 58%. In order to ascertain the true improvement in efficiency due to the mirror we will have to wait until a stack can be deposited on a planarized backplane.

4. PLANARIZATION

A certain amount of circuitry is necessary at each pixel in order to obtain the high-speed multi-level modulation. The methods used to generate these circuits result in uneven surface layers due to the circuit topology. These uneven surfaces cause a considerable amount of light to be diffracted. Additionally, VLSI techniques result in other optical quality issues including local flatness variations and global warpage. Therefore, the VLSI metal is primarily a diffuse scatterer, which reduces the light-efficiency and the contrast. Integrated circuit fabrication processes result in devices exhibiting excellent electrical performance, but poor optical quality. Planarization is necessary to overcome backplane optical losses.

One method to accomplish planarization is to utilize chemical-mechanical polishing (CMP) of a thick oxide layer to remove surface variations (see Figure 8). The CMP method involves front surface polishing on a state-of-the-art cassette-to-cassette process tool. Beginning with unpassivated die, a conformal oxide coating is deposited. The oxide is polished back to within a submicron distance of the underlying pixel pads. At this point the surface is optically flat. Following the oxide polish, a dielectric stack can be deposited to enhance reflectivity. Another possible top surface is a metal mirror. However, this requires vias to be etched to each of the underlying pixels, then lithography of the topmost metal surface.

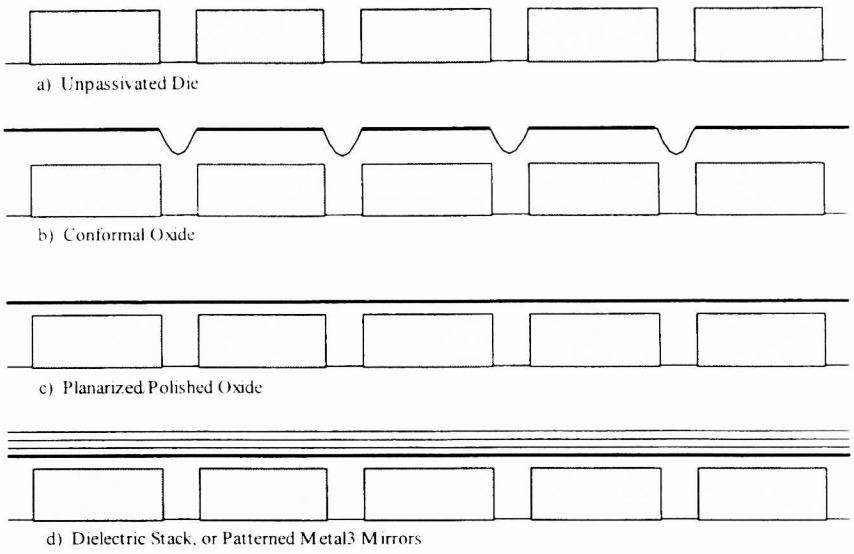

Figure 8. Steps required for planarizing the VLSI die.

5. SUMMARY AND CONCLUSIONS

A liquid crystal on VLSI silicon optical phased array as shown in Figure 9 has been discussed. A prototype backplane and the updated version currently in fabrication are specified. The liquid crystal modulator characteristics are presented. The optical diffraction properties of the prototype backplane and liquid crystal optical phased array are examined experimentally. Preliminary results indicate that the key to successful implementation of a liquid crystal optical phased array will be the caliber of the backplane in terms of its optical quality.

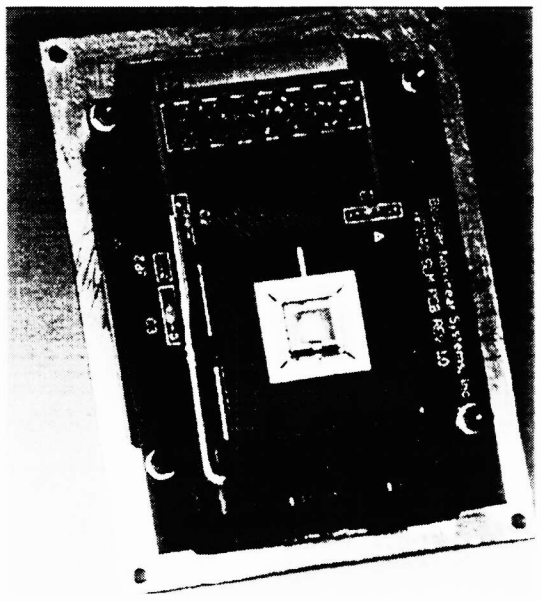

Figure 9. The optical head and amplifying circuitry for the VLSI liquid crystal optical phased array. The device is shown with the front housing cover removed. For a complete system, this unit is interfaced with a driver board residing in a desktop PC.

6. ACKNOWLEDGMENTS

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