256 × 256 liquid-crystal-on-silicon spatial light modulator

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A 256 × 256 pixel spatial light modulator (SLM) is designed and constructed by the use of liquid-crystal-on-silicon technology. The device is a binary electrically addressed SLM with a measured zero-order contrast ratio of 70:1 and an imaged contrast ratio of 10:1. The pixel pitch is 21.6 μm, which gives an array size of 5.53 mm. The electronic load time is 43 μs, and the 10%-90% switching time of the liquid crystal is ~75–80 μs at room temperature, which implies a maximum frame rate of ~8.3 kHz. We discuss the design trade-offs that are intrinsic to this type of device and describe how the primary application for the device in an optical correlator influenced the final design.

1. Introduction

A spatial light modulator (SLM) is a device that can impress information on an optical wave front. An electrically addressed SLM translates information from the electronic domain to the optical domain. The applications for SLM's are numerous; they include coherent optical processing applications, data routing, data input to optical processing systems, and information display.

Spatial light modulation can be accomplished by electro-optic, acousto-optic, magneto-optic, mechanical, photorefractive, optical absorption, and interference effects in a variety of materials. The advantages of liquid-crystal (LC) materials for SLM's include their high birefringence and low-voltage operation. These properties permit large optical effects to be induced in LC layers a few wavelengths thick. The low-power operation of the LC materials permits large arrays to be constructed to operate at gigabit per second data rates, even though the individual pixels switch in the tens of microseconds time scale. The integration of LC's with silicon backplanes has been a primary technology for research in smart pixel devices as detectors, electronic logic, and modulators are readily integrated into a single device.

In this paper we present a discussion of the design issues inherent to electrically addressed VLSI–ferroelectric liquid-crystal (FLC) SLM's, we describe the SLM that we fabricated, and we present and discuss the first experimental results from the device.

2. Spatial Light Modulator Design

A. Device Description

This SLM is of the class of devices that are often described as DRAM devices because they contain a single transistor at each pixel. In fact, their similarity to active-matrix displays is closer.

Each pixel is addressed by a (column) data wire and a (row) select wire. Each pixel contains a transistor that controls the flow of charge from the data wire to the pixel mirror under the control of the select (or gate) wire.

We construct the SLM by sandwiching a thin layer of LC between a silicon integrated circuit and a piece of glass coated with a transparent electrode. The optical modulating portion of the chip is a square array of mirror/electrodes that are electronically programmed to either 0 or 4.6 V (V_{dd} - V_{thresh}, V_{dd} = 6 V). The voltage of the cover-glass electrode is maintained midway between these two values such that opposing polarity electric fields can be applied across the LC layer.

B. General Design Trade-Offs

Because there are trade-offs that are intrinsic to the design of this type of SLM, it is clear that the best
devices must be, to some extent, application specific. The basic design trade-offs are

1. Pixel patch versus fill factor. The fill factor is often defined as the fraction of the array that comprises the addressable metal mirror. This can be increased either by the use of a smaller geometry silicon fabrication process or by an increase in the size of the pixel so as to reduce the proportion of area taken by gaps between the mirrors. For some applications the fill factor is a more useful parameter to maximize, as this is the fraction of the array that is addressable and also reflects at the same phase and so contributes directly to the zero-order output replica in the Fourier plane.

2. Pixel size versus diffraction scaling factors, electronic address times, cost, and flatness. Although large pixels have larger fill factors, the resulting scaling factors introduced in diffraction-based applications are likely to increase. Furthermore, large pixels are more difficult to address rapidly with standard polysilicon address lines, cost more to fabricate, and the resulting large die is less likely to be flat.

3. Light shielding and pixel complexity versus fill factor. The flat fill factor is maximal for simple pixels; flatness can be traded for other advantages, though. For example, there are advantages in using memory circuitry at each pixel and this can be hidden under the second-level metal at the cost of flatness. It is also possible to overlap the first- and second-level metal layers to achieve almost complete light shielding, but again only by reducing the flat fill factor. In the case of the SLM described here, implementation of complete light shielding would cause a reduction of the flat fill factor from 60% to ~36%.

4. Pixel capacitance can be increased by implementing a thin-oxide (or metal-oxide semiconductor) capacitor at each pixel. The reasons for doing this are twofold: one is to help under the circumstances in which the illumination intensity is large enough to induce photocurrents of sufficient magnitude to drain the pixel capacitance of significant charge before the next refresh. Either high levels of illumination or low refresh rates can lead to this. The other reason is to help with fast switching of high spontaneous polarization FLC materials. These materials are expected to be faster switching as the switching time is proportional to $1/P$. The disadvantages are that the flat fill factor is reduced, the minimum cell thickness is increased, and the increased capacitance requires more power dissipation to drive. Thin-oxide capacitors have been used on a similar device.

3. Spatial Light Modulator Design for an Optical Correlator Application

A. Specifications

The SLM described in this paper was designed specifically for an optical correlator, which uses this device in both the input and the Fourier planes. The SLM specifications that are of most interest in this application are speed, optical efficiency, and pixel pitch.

1. Speed

A high frame rate is important for achieving a high computation rate. Both the electronic load time and the LC switching time contribute to the frame time and, in a device of this size, both are similarly important to the ultimate frame rate achieved. $\tau_{\text{frame}}$, the minimum time between optically valid frames, is calculated by adding the time taken to load all pixels with data ($\tau_{\text{load}}$) to the time taken for the FLC to switch ($\tau_{\text{FLC}}$):

$$\tau_{\text{frame}} = \tau_{\text{load}} + \tau_{\text{FLC}}$$

This is the time taken to switch the LC plus the time between the first and the last rows of the array being addressed. If there is a delay in the optical response of the FLC after it is electrically addressed, then it does not affect the frame time if the delay is short compared with the electrical load time, $\tau_{\text{load}}$. If a delay existed that was comparable with the load time, then the FLC could be addressed with new data before complete switching had occurred.

2. Optical Efficiency

Optical efficiency is an important parameter because we need enough light in the output plane to permit detection of the signal at high speed with a moderate source power. The flat fill factor is important because it determines how much energy is in the zeroth-order replica of the transform of the data. If we assume that the total useful signal output from the SLM is proportional to the fill factor then this (along with the efficiency of the LC configuration and the reflectivity of the pixel mirrors) tells us how much energy, in total, is in all the replicas of the transform of the data. The envelope function that describes how this energy is distributed among the replicas is the square of the Fourier transform of the function describing a single pixel. Clearly, smaller pixels spread a greater proportion of the signal into higher orders, further reducing the energy in the zeroth-order replica. Mathematically the Similarity theorem of Fourier transforms describes this situation.

A reasonable model for a flat-mirror pixel function is a two-dimensional rect function $[\text{rect}(x/m_x) \times \text{rect}(y/m_y)]$ whose width equals the width of the active mirror. Assume a fixed pixel period and consider what happens as we shrink the size of the mirrors by a factor $a$, in one dimension first.

If we consider first a fill factor of 100%, the zeros of the transform of the pixel rect function fall exactly on the position of the output replicas. All the energy is therefore in the zeroth-order replica. As the fill factor is reduced, the envelope function $[\text{the transform of the pixel}]$ spreads. Energy begins to appear in the higher-order replicas, and the power in the zeroth order is diminished in proportion to $a^2$. 

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Shrinking the mirror in both x and y reduces the power by a factor of \( a^4 \), which is equivalent to the fill factor squared.

Thus the power in the zeroth-order replica of the transformed output of the SLM is proportional to the flat fill factor squared. Cascading two identical devices in a correlator results in the output power at the detector being proportional to the flat fill-factor to the fourth power. Clearly, care is required when SLM's are designed for correlator application as a not unreasonable flat fill factor of 50% implies a maximum throughput of only 6.25%.

3. Pixel Pitch

The pixel pitch is related to the focal length, \( f \), of the Fourier-transform lenses used in the correlator by the relationship

\[
f = \frac{Na^2}{\lambda},
\]

where \( N \) is the number of pixels across the array, and \( a \) is the pixel pitch. A small pixel pitch requires short focal lengths that are easier to implement in a compact package. The SLM described in this paper has \( N = 256 \), \( a = 21.6 \, \mu m \), and when used in a correlator illuminated by a laser diode (\( \lambda = 830 \, nm \)), would require lenses with a 14.4-cm focal length.

B. Device Description

1. Pixel Design

The final choice of 21.6 \( \mu m \) for the exact pixel pitch was made because it is a suitable compromise for the correlator application between throughput and system size. It also allows this SLM, when illuminated by a \( \lambda = 830 \, nm \) laser, to be inserted directly into a correlator that was designed for a 128 \( \times \) 128 VLSI/FLC SLM. 10

The pixel was designed to have as large a flat fill factor as possible in the 1.2-\( \mu m \) minimum linewidth technology used. Standard silicon chip fabrication processes include a protective layer through which holes must be etched to gain access to the metal layers. Because of constraints on the size of these etch holes, the fill factor would be reduced if this layer was used. For example the 128 \( \times \) 128 VLSI/FLC SLM described in Refs. 2 and 10 has 30-\( \mu m \) pixels, but the protective passivation layer forces the fill factor to be reduced to \( \sim 30\% \). By having the chips used in this SLM fabricated without the overglass layer, we achieved a total fill factor of 79% and a flat fill factor of 60%. This design uses minimum-size first-level metal wires for the data lines and minimum-size polysilicon wires for the select lines. The use of polysilicon select wires has implications for the addressing scheme, as there is a significant propagation delay in the gate line. This is discussed in Subsection 3.B.2.

A thick-oxide pixel capacitor was used for two reasons. First, to maximize the flat fill factor, which for our application is important, and second, to allow us to construct thin LC cells on the silicon backplane. We estimate the value of our pixel capacitance to be \( \sim 50 \, pF/pixel \).

2. Addressing Scheme

Data are presented to the device through 32 parallel electronic input lines. These 32 inputs are converted into 256 inputs for the pixel array by clocking each input into an 8-bit shift register. After eight clock cycles, the data are presented to the array data wires, where they are available to be sampled and held on a row of pixels under the control of the appropriate select wire. The data are on-chip buffered to facilitate high-speed addressing of the array. This is done in such a way that the relatively slow switching of the polysilicon select lines happens in parallel with the loading of the data shift registers, thus permitting the frame to be loaded in a continuous stream of 2048, 32-bit words. All the internal control signals required for doing this are on-chip generated from a single input clock and a frame synchronization pulse. The select wires that drive the pixel transistor gates are controlled by a 256-bit shift register that passes a single token down the side of the array to activate a single row of the array at a time. This select shift register is duplicated on both sides of the array to facilitate high-speed addressing and also to improve device yield through circuit redundancy. We have shown that this also allows one to fabricate a working SLM should one of the 256-bit shift registers be damaged during assembly. We test the main addressing circuits by setting the chip in a test mode and monitoring test points. This allows selection of good candidate chips for the subsequent filling process. The yield of good candidates from the integrated-circuit fabrication and bonding processes appears to be \( \sim 70\% \). It is not yet known how the success of the address testing of a candidate serves to identify a chip that has every pixel working correctly.

3. Assembly and Filling

We make VLSI/FLC SLM's by sandwiching a thin layer of FLC between a flat cover glass and the silicon chip. The cover glass is coated with an indium tin oxide transparent electrode and then with a thin layer of polyvinyl alcohol that acts as an alignment layer. The glass and the die are separated by evenly dispersed polyimide spheres, providing the gap for the LC mixture. The spheres have a nominal diameter of 1.3 \( \mu m \) and are spun on in an alcohol solvent. A jig is used to position the glass accurately over the die before it is finally glued in place. The assembly is heated in a vacuum until the LC is isotropic and the cell is filled by capillary action with the LC mixture BDH SCE13. 11 One side of the cover glass is coated with chrome that overlaps the indium tin oxide and provides a contact to the transparent electrode.
4. Experimental Results

A. Electrical Results
We have addressed the SLM at clock rates of as high as 48 MHz with arbitrary frames of data from our electronic driver board. Because of the way the on-chip clock generator is used, a 32-bit word is input on each clock cycle. At this data rate (\(1.5 \times 10^9\) bits/s), a frame is loaded in 43 \(\mu\)s, an image refresh rate of 23 kHz. We plan to use a printed circuit board that should allow us to achieve faster address rates, as simulations suggest that the silicon backplane will function at speeds of at least as high as 80 MHz.

The on-chip clock and control signal generation simplify the programming of the SLM from a PC. We have also addressed the SLM from a simple 32-bit input–output board on an IBM-compatible PC. This can output data at a 200-kHz clock rate, which gives \(\sim 130\) frames per second refresh on the SLM. This computer was used to address the SLM for all the optical experiments described below, except whether otherwise indicated.

B. Optical Results
Figures 1 and 2 are photomicrographs of images displayed on the SLM and imaged onto a 35-mm camera by an Olympus SZH10 microscope that illuminates the SLM with light from a tungsten halogen bulb. We estimated the thickness of the FLC modulating layer with a SPEX spectrometer. The results suggest that the cell is zero-order half-wave retarder in reflection at \(\lambda = 700\) nm. This is consistent with a cell thickness of \(\sim 1\) \(\mu\)m. This datum is supported by qualitative observations of the device. In the on state the image appears a fairly neutral white, rather than the more saturated color typical of a thicker device.

Note that this cell thickness is comparable with the thickness of the layers used in silicon chip fabrication. This cannot be readily achieved if thin-oxide pixel capacitors are used, as the thin-oxide layer would significantly reduce the height of the mirrors below the rest of the chip structure. To do so would require extra processing steps that were not considered necessary for this project.

1. Contrast Ratio
Contrast ratio is often defined in terms of the on–off intensity ratios in an image of the SLM. For the correlator application, a more useful measure is the contrast in the zeroth-order replica in the Fourier-transform plane. Much of the lower contrast noise is outside the bandwidth of the correlator system. This zero-order contrast ratio can be measured quite easily and yields a higher value than the contrast ratio measure obtained when the imaging condition is used. It is actually more difficult to make an accurate measurement of the imaged contrast as some of the higher spatial frequencies are inevitably lost in the imaging system. In the device described in this paper, the image contrast ratio at \(\lambda = 633\) nm from a spot \(\sim 2\) mm in diameter is 10:1, and the zero-order replica contrast is 70:1. The imaged contrast ratio includes the contributions from the space between pixels. Imaging a single pixel mirror would probably yield a result close to the 70:1 zero-order contrast. This measurement was made at a 130-Hz refresh rate with low power illumination and alternately on and off images each present for several seconds to facilitate measurement with an optical power meter. Photoinduced leakage of charge from the pixels leads to a reduction in contrast ratio. In a separate experiment an SLM was driven with a driver board clocked by a 35-MHz crystal that corresponds to a frame refresh rate of \(\sim 27.1\) kHz. The on state was examined for the sawtooth modulation characteristic of photoinduced discharge. At this refresh rate no modulation of the on state was seen until the illumination intensity reached \(\sim 29\) mW/cm\(^2\) (\(\lambda = 633\) nm). At the maximum output of our laser diode we could illuminate the pixel array with 9.5 mW (31.4 mW/cm\(^2\)). This intensity caused a rounded sawtooth modulation in the on state with a depth that was 12% of the maximum signal.
2. Switching Speed

We measured the potential switching speed of the SLM LC layer by imaging a single row of pixels onto a slit and detecting the transmitted light. Because all the pixels in a row receive new data on the same clock cycle, an accurate measurement of the LC switching time can be made. Figure 3 is a record of an oscilloscope trace that shows the 10%-90% rise time, which was measured at room temperature, to be ~50 μs. This fast switching is consistent with a thin LC layer. By imaging the top row of the SLM, we could measure the delay between the pixel being addressed and the FLC optical response to the applied field. These pixels receive their data on the eighth clock cycle, and so from Fig. 4 we can estimate a delay of ~15 μs. This measurement was made with the transparent electrode at the same voltage that was used for both the rise- and the fall-time measurements.

It should be noted that when we address the SLM from the personal computer, the gate wires are, in general, active for approximately 10 μs while valid data exists on the data wires. However, in this particular experiment, the form of the data meant that the pixels were driven with the new data for ~40 μs. This is because adjacent rows were all being written with the same data. In effect these pixels are being driven with a voltage source for a large fraction of the total delay plus switching time (~65 μs). When the SLM is loaded at a high refresh rate from the driver board, the pixel is exposed to the data line for less than a microsecond, much less than the response time of the LC. This requires the LC to use the charge stored on the pixel to switch. Under stored charge switching, we may expect to find that the FLC switches more slowly than when switched with a constant voltage. This is because the FLC polarization charge neutralizes some of the stored charge, and the switching time \( \tau \) is inversely proportional to the applied field. As the FLC switches, this field is reduced.

We investigated the differences between constant-voltage switching and stored charge switching by using a driver board fitted with a 35-MHz crystal, yielding a 17.1-KHz electronic refresh rate. This board is hard wired for the correlator application to write 10 positive frames followed by 10 inverse frames, so preserving dc balance and so preventing ionic degradation of the LC cell. In normal use this driver board addresses the SLM in a true stored charge switching mode, but we can arrange for it to drive the SLM in a mode that gives constant-voltage switching for the purposes of this experiment. We clamped the input to the gate shift registers high, which means that all the gate wires were continuously active. A sequence of alternately all-on and all-off images were written to the SLM. This addressing mode loads the array data-wire drivers much more heavily than they were designed for, but simulations show that they can switch the data wires in less than 1 μs, which is amply fast enough for this experiment. By imaging a small area of the array onto the detector and switching from conventional addressing to constant-voltage addressing, we can observe the differences in the optical response of the LC.

Figure 5 presents the results of such an experiment. We generated these traces by making no changes in

![Fig. 3.](image) (a) Oscilloscope trace record of the optical rise time of the FLC layer in the SLM. The 10%-90% rise time is 50 μs. (b) Oscilloscope trace record of the optical fall time of the FLC layer in the SLM. The 90%-10% fall time is 50 μs.

![Fig. 4.](image) Oscilloscope trace record of the response of the first row of pixels on the SLM shown with the input clock waveform. The pixels receive their electrical signal on the eighth short clock pulse. The delay between the electrical stimulation and the 10% level of the optical response of the pixels can be estimated to be ~15 μs.
plane losses by shining a ($\lambda = 633$ nm) He–Ne laser beam on a bare silicon chip and measuring the fraction of the incident power that was reflected in the zero order. This experiment gave a result of 13.5%. This is consistent with the result of the device reported in Ref. 7, which has a similar flat fill factor, although it has a 30-$\mu$m pixel pitch.

The second experiment was done on the assembled SLM in conjunction with the contrast ratio measurements. The device was illuminated with polarized He–Ne light, and the output was viewed through a polarizer crossed with the input light. As much of the output light as possible was collected to give an accurate estimate of both the imaged contrast ratio and the optical efficiency. Approximately the center ±1 diffracted orders were collected in the imaging system. Of this output light, 15% was in the zero order. The third experiment was to measure the output in the zero order in the on state as a fraction of the incident light when the SLM was configured for maximum contrast. The result of this experiment was that 3.4% of the incident light appears in the zero-order output. Table 1 summarizes these results along with the most recently published results from other groups reporting similar devices, although there may be more current results reported elsewhere in this special issue of Applied Optics.

4. Application in an Optical Correlator

Two of our SLM’s have been used in an optical correlator as input- and Fourier-plane devices operating in a binary-phase mode. An 830-nm laser diode was used as the source, and a Pulnix TM-7EX CCD camera was used as the output-plane detector. The system was operated at 1000 correlations per second, i.e., a positive input and filter plane pattern were written for 500 $\mu$s, followed by their inverses for 500 $\mu$s. The camera shutter was set at 1 ms to capture the output from both the true and the inverse frames.

On-axis and off-axis inputs consisting of small target images that used 0.6 to 1% of the pixels in the input array were used. With the laser output set to approximately 5 mW the correlation peaks in the output were able to saturate the camera and yield a signal-to-noise ratio (peak/rms) of greater than 10 dB for most of the images.

5. Power Dissipation in Actively Addressed Spatial Light Modulators

A. Power Dissipation in Switching the FLC

Because low power dissipation is an advantage of LC-based devices, we discuss here the intrinsic power dissipation routes that exist in the single transistor style of VLSI-based FLC SLM’s.

The switching energy that is dissipated in a unit area FLC layer is $2PV$, where $P$ is the spontaneous polarization of the FLC, and $V$ is the applied voltage. This energy is intrinsic to the light modulation material and is related to the shortest achievable
Table 1. Comparison of Our Results with the Most Recently Published Results from Other Groups Working on Similar Devices

<table>
<thead>
<tr>
<th>Parameter</th>
<th>CU/BNS(^a)</th>
<th>EU/BNR/GEC (Ref. 12)(^b)</th>
<th>Displaytech (Ref. 7(^d))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array size</td>
<td>256 x 256</td>
<td>176 x 176</td>
<td>256 x 256</td>
</tr>
<tr>
<td>Pixel pitch ((\mu m))</td>
<td>21.6</td>
<td>30</td>
<td>30 (20)</td>
</tr>
<tr>
<td>Fill factor (%)</td>
<td>79</td>
<td>79</td>
<td>90 (72)</td>
</tr>
<tr>
<td>Flit fill factor (%)</td>
<td>60</td>
<td>28</td>
<td>58 (16)</td>
</tr>
<tr>
<td>Backplane optical efficiency (%)</td>
<td>13</td>
<td>NA</td>
<td>13 (0.6)</td>
</tr>
<tr>
<td>Frame load time ((\mu s))</td>
<td>43(^f)</td>
<td>28(^g)</td>
<td>25(^h)</td>
</tr>
<tr>
<td>LC</td>
<td>BDH SCE13</td>
<td>BDH SCE13</td>
<td>Merck ZLI-3654 (NA)</td>
</tr>
<tr>
<td>Contrast ratio</td>
<td>70:1 (10:1)(^i)</td>
<td>NA</td>
<td>29:1 (NA)</td>
</tr>
<tr>
<td>LC switching time ((\mu s))</td>
<td>50</td>
<td>NA</td>
<td>225 (NA)</td>
</tr>
<tr>
<td>Frame rate (kHz)</td>
<td>~10 (room temp.)</td>
<td>NA</td>
<td>4</td>
</tr>
</tbody>
</table>

\(^a\)More recent results may appear elsewhere in this issue of Applied Optics.

\(^b\)Colorado University/ Boulder Nonlinear Systems.

\(^c\)Edinburgh University/ BNR Europe Ltd./ GEC-Marconi Research Centre.

\(^d\)Ref. 7; two generations of devices are described in Ref. 7. The specifications of the first-generation device are shown in parentheses.

\(^e\)NA, not applicable.

\(^f\)Driver board limited.

\(^g\)It is implied, although not stated, in Ref. 13 that this time is limited by the driver board.

\(^h\)Ref. 7: two generations of devices are described in Ref. 7. The specifications of the first-generation device are shown in parentheses.

\(^i\)Zero-order contrast, and 10:1 is imaged contrast.

\(^j\)This contrast ratio measurement was made by imaging through a grid, thereby removing the effect of the gaps between the pixels. This measurement is similar to the zero-order contrast ratio measurement described in this paper.

The switching time\(^12\) of the FLC through the relation

\[ t_s = \left( \frac{3.6 \pi d^2}{U} \right)^{1/2}, \tag{3} \]

where \(\eta\) is the viscosity of the material, \(d\) is the cell thickness, and \(U\) is the power dissipation in the material. Some comments should be made about this relationship. It refers to the intrinsic material properties and takes no account of the driving schemes that are used. This affects the results in two ways.

First, the driving scheme may invalidate the assumptions used in this estimate of switching energy. Second, it is inappropriate to consider the material switching energy in isolation. The energy dissipated in the driving scheme should be considered because it is intrinsic to this type of device that this power will be dissipated on the silicon backplane.

To consider the first point, the expression \(E = 2PV\) assumes that the FLC is switched in a cell that is driven with a potential difference across the plates that switches from \(+V\) to \(-V\) (or vice versa), and then remains constant through the duration of the switching. In the SLM this may or may not be true, depending on the regime of operation. In one extreme case, the pixels are addressed relatively slowly compared with the switching time of the FLC such that the FLC is exposed to the constant applied voltage for the duration of its switching. In this case the above expression for material power dissipation is valid. This mode of addressing does not make use of the speed increase available through use of an active backplane compared with passively addressed devices, and so it is not generally considered to be desirable. In the other extreme case the pixel is charged to \(V\), for example, and is isolated from its data wire in a time that is short compared with the FLC response. The FLC then switches by using the field provided by the charge stored on the pixel. As it switches, the polarization currents reduce the voltage across the FLC layer. Less energy is dissipated in this case. One can write the energy dissipation as

\[ E = 2P(V + V')/2, \tag{4} \]

where \(V'\) is the final voltage across the cell, which in turn can be approximated by

\[ V' = V - 2P/C_{pixel}. \tag{5} \]

In practice, a device may well be operating somewhere between the two extreme cases described.

Typically, as we show below, the material switching energy is low compared with the energy dissipated in driving the pixels, not just in driving the pixel capacitances themselves, but in driving the data wires as the loading presented by them can be larger, in this particular device by a factor of \(\sim 20\).

B. Data Dependence of Frame-Write Energy

The energy dissipated in writing a frame is strongly data dependent. Data that require all the array data-wire voltages to be changed between each two succeeding rows cause most power to be dissipated. An example of such a pattern is a fine checkerboard or a pattern of alternating horizontal lines (with the data wires running vertically). Negating the entire image is not intrinsically highly dissipative unless the data are of the form described above.

The total energy dissipated in writing a frame can
be written as

$$E = NV^2C_{\text{SelectWire}} + FA\left(2PV_{\text{eff}} + \frac{1}{2}C_{\text{pix}}V_{\text{pix}}^2\right) + \frac{1}{2}GN^2C_{\text{DataWire}}V^2,$$

(6)

where

- $V$ is the chip supply voltage;
- $V_{\text{pix}}$ is the voltage swing that can be applied to the pixel. Usually $V_{\text{pix}}$ is equal to $V$, minus the threshold voltage of the pixel transistor;
- $N$ is the number of rows in the array, assuming an $N \times N$ SLM;
- $F$ is the fraction of pixels that have their state changed during the frame-write operation;
- $C_{\text{SelectWire}}$ is the capacitance of the row select wire, including pixel transistor gates;
- $A$ is the area of the switchable FLC in the array, i.e., the total area multiplied by the fill factor;
- $P$ is the spontaneous polarization of the FLC;
- $V_{\text{eff}}$ is the effective switching voltage seen by the FLC. The value of this voltage depends on the addressing regime. Recall that the cover glass is maintained at a voltage midway between the lowest and the highest voltage that can be applied to the pixel. Thus $V_{\text{eff}}$ can range from (in the slow case) $V_{\text{eff}} = V_{\text{pix}}/2$ to (in the fast case) $V_{\text{eff}} = V_{\text{pix}}/2 - 2P/C_{\text{pix}}$ [from Eq. (5)];
- $C_{\text{pix}}$ is the capacitance per unit area of the pixels. This includes a contribution from the mirror to the substrate and from the mirror to the cover glass;
- $G$ is the data transition fraction, i.e., the number of data-wire transitions required for writing the frame divided by $N^2$, the maximum number of data-wire transitions possible;
- $C_{\text{DataWire}}$ is the capacitance of the data wire, including pixel transistor drains.

The first term in Eq. (6) is due to the select wires each being switched to address the array. This contribution is usually small compared with the third term. The second term is the contribution that is due to the number of pixels that undergo a transition in the frame-write operation. The third term is the contribution that is due to the switching of the data wires.

Some approximations are contained in Eq. (6):

(1) The use of the parameter $F$ in Eq. (6) neglects a correction that should be made to account for top-up charging of a pixel that was switched (in the fast mode) during the previous frame. If this pixel is to remain in the same state on this frame, then charge will flow through the pixel transistor to replenish the charge neutralized by the FLC polarization charge.

(2) There is no account taken of the recharging of pixels that have become partially discharged through photoinduced leakage (but that are not being switched, so far as the data are concerned).

(3) Equation (6) assumes a certain timing relationship between the data-wire update and the select-wire activation. It is assumed that the data wires are set with data, and then the appropriate row select wire is pulsed high, then low. In fact, a better scheme is to send the gate wire high before, or during, the transition of the data wires to the valid voltages for the pixels that are being addressed. This scheme has a timing advantage, but it means that some pixels will momentarily be set to the wrong value. Typically the duration of this glitch will be too short for the FLC to switch. The pixels that are affected are those that are being set to the same value as in the previous frame and that have the corresponding pixel on the previous row set to the opposite value. Each of these pixels contributes an extra $C_{\text{pix}}V_{\text{pix}}^2$ to the total.

These approximations all pertain to the pixel-dependent part of Eq. (6); as such, their effect is relatively small for this device and so, for the sake of brevity, we note their existence without including them in the examples presented below.

To give a feeling for the relative magnitudes of the terms in Eq. (6) in the SLM described in this paper we can consider a few example image transitions.

The examples are tabulated in Table 2 and are

<table>
<thead>
<tr>
<th>Example Case</th>
<th>Data Transition Fraction, $G$</th>
<th>Term 1 (nJ)</th>
<th>Term 2 (nJ)</th>
<th>Term 3 (nJ)</th>
<th>Total Energy (nJ)</th>
<th>Power at 10 kHz (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) Refresh simple</td>
<td>0</td>
<td>6</td>
<td>0</td>
<td>0</td>
<td>6</td>
<td>0.06</td>
</tr>
<tr>
<td>(2) Invert simple</td>
<td>0</td>
<td>6</td>
<td>62</td>
<td>3</td>
<td>72</td>
<td>0.7</td>
</tr>
<tr>
<td>(3) Write horizontal stripe</td>
<td>1</td>
<td>6</td>
<td>31</td>
<td>852</td>
<td>890</td>
<td>8.9</td>
</tr>
<tr>
<td>(4) Refresh horizontal stripe</td>
<td>1</td>
<td>6</td>
<td>0</td>
<td>852</td>
<td>858</td>
<td>8.6</td>
</tr>
<tr>
<td>(5) Invert horizontal stripe</td>
<td>1</td>
<td>6</td>
<td>62</td>
<td>852</td>
<td>920</td>
<td>9.2</td>
</tr>
<tr>
<td>(6) Invert vertical stripe</td>
<td>1</td>
<td>6</td>
<td>62</td>
<td>3.3</td>
<td>72</td>
<td>0.7</td>
</tr>
<tr>
<td>(7) Write binarized natural scene</td>
<td>0.2</td>
<td>6</td>
<td>62</td>
<td>31</td>
<td>170</td>
<td>2.1</td>
</tr>
<tr>
<td>(8) Write dithered image</td>
<td>0.33</td>
<td>6</td>
<td>31</td>
<td>251</td>
<td>318</td>
<td>3.2</td>
</tr>
</tbody>
</table>

*The numbers in this column correspond to the explanations given in the text in Subsection 5.8 for these cases.*
(3) Switching from an all-off image to a fine horizontal stripe image. \( F = 0.5, G = 1, E = 890 \, \text{nJ} \).

(4) Refreshing a fine horizontal stripe image. \( F = 0, G = 1, E = 858 \, \text{nJ} \).

(5) Inverting a fine horizontal stripe. \( F = 1, G = 1, E = 920 \, \text{nJ} \).

(6) Inverting a fine vertical stripe. \( F = 1, G = 0.004, E = 72 \, \text{nJ} \).

There is a large factor of difference between the energy dissipated in writing the simple images and the high write-energy images. This is interesting because the last two examples compare the same image, rotated through 90°. If an application uses data of a known form, it may be that one orientation of the device is advantageous if power dissipation is to be minimized.

It is interesting to consider where in this range the energy required for writing a typical image lies. We can consider one type of image here. There is evidence to suggest that in natural environment scenes, the power spectrum falls off at \( 1/f^2 \), where \( f \) is the spatial frequency in the scene.\(^{15}\) This is justified partly by experiment and partly on the basis of scale invariance in natural image power spectra. This result allowed us to generate images with these statistics and to calculate transition numbers for this kind of scene. When this type of image is binarized with a threshold at the median pixel level, which was chosen to preserve information,\(^{16}\) the transition fraction \( G \) is \( \sim 0.2 \). If a dithered representation of the same scene is used, then the transition fraction increases to 0.5. This is to be compared with the dithered test image written to the SLM (see Fig. 1) that has a transition fraction of 0.33. When this image is binarized, the transition fraction drops to 0.03, which is consistent with the observation that this test image has a large low-frequency content.

There are other sources of power dissipation on the chip such as input pad drivers, clock generation, and shift registers. These have not been considered in this analysis as they are less fundamental than the dissipation that is intrinsic to driving the array modulating material, pixels, and addressing wires.

The conclusion of this analysis is that the energy dissipated in writing an image on our device is strongly dependent on the image data and is more than an order of magnitude greater than the dissipation that is due to the FLC material properties. It should be noted that thin-oxide pixel capacitors increase the pixel capacitance to a similar value to the data wires,\(^{7}\) shifting the emphasis away from the third term in Eq. (6) because the pixel capacitance in the second term is increased by over an order of magnitude. In this case, frame inversion becomes a high-energy operation for all data.

6. Conclusions

In conclusion, we have successfully designed and fabricated a \( 256 \times 256 \) LC-on-silicon SLM for an optical correlator application. The silicon backplane functioned correctly at 48 MHz on the first iteration of the chip design. On-chip clock and control generation facilitate data loading at a rate of one 32-bit word per clock cycle, leading to an input data rate of \( \sim 1.4 \, \text{Gbits/s} \) and an aggregate data rate of \( \sim 0.54 \, \text{Gbits/s} \). The switching speed of the LC was measured to be \( \sim 75-80 \, \mu s \) at room temperature. We measured the contrast ratio to be 70:1 in the zero-order and 10:1 imaged. The switching speed and color of the on-state are consistent with a cell of \( \sim 1-\mu \text{m} \) thickness. The silicon backplane was successfully designed specifically so that a thin cell could be fabricated.

We have discussed the design issues specific to the single-transistor LC-on-silicon SLM, including those that are most important to optical correlators. We have analyzed the power dissipation inherent to this type of device and shown that, for our SLM, the form of the data is important.

Future work will concentrate on improving the optical quality of the devices. Specifically, we anticipate improving the contrast ratio by using a two-sided SiO\(_2\)/LC alignment. We plan to determine the highest operating clock speed of the chip. Simulations suggest that it will run at 80 MHz, giving a 25-\( \mu \text{s} \) frame refresh, but this has yet to be demonstrated in practice.

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References


11. British Drug House mixtures are available from Merck Ltd., Westquay Road, Poole BH15 1HX, UK.


