High-speed multi-level 512x512 spatial light modulator

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ABSTRACT
Recent advancements in our high-speed multi-level (analog) 512x512 liquid crystal Spatial Light Modulator (SLM) will be presented. These advancements include smaller pixel pitch, greatly improved optical efficiency, and higher speed operation. The new VLSI SLM can utilize Ferroelectric Liquid Crystal (FLC) or Nematic Liquid Crystal (NLC) to achieve phase-only, amplitude-only, and phase-amplitude-coupled modulation. This device has applications in optical processing, optical storage, holographic display, and beam steering. Design criteria and experimental data will be presented.

Keywords: Spatial light modulator, liquid crystal, optical correlator, optical processing, beam steering, holography

1. INTRODUCTION
Boulder Nonlinear Systems (BNS) has made, and will continue to make, several advances in all components of our liquid crystal Spatial Light Modulator (SLM) technology. These include two new versions of our 512x512 multi-level SLM, one has the same pixel pitch as the original device, and the second has a much smaller pitch. The focus for the design of the small pitch device was towards developing small optical correlators, while the focus for the new large pitch device was towards projection display. While neither device is limited in use to these particular applications, some design elements lend themselves better to certain applications. For instance the large pixel pitch and high fill factor are better suited to projection display, while a small pitch SLM allows smaller optical correlators, and lower fill factor yields improved spatial frequency response in an optical correlator.

2. ORIGINAL 512 X 512 MULTI-LEVEL SLM
The original BNS 512x512 multi-level SLM is based on a 5-volt silicon backplane integrating both high-density electronics and the reflective pixel pads. The silicon backplane is mounted in a ceramic Pin Grid Array (PGA) package with wire bonds to make electrical contact. The backplane is then covered with a glass window to form a precise uniform gap between the backplane and the window. This gap can then be filled with either Ferroelectric Liquid Crystal (FLC) or Nematic Liquid Crystal (NLC) to achieve the desired optical modulation effect. Figure 1 shows a picture of an original 512x512 multi-level SLM. Figure 2 shows sample images from a 512x512 FLC SLM and Figure 3 shows sample images from a 512x512 NLC SLM.

The original device has 512x512 pixels with a 15-µm pitch for a total active area of 7.68x7.68-mm. The fill factor of each pixel is approximately 60%, however due to the relative ratio of the pixel pitch to the silicon foundry process size much of the pixel pad has varying underlying structures. These underlying structures combined with the conformal nature of each layer of the process results in much of the pixel pad being quite rough, diffracting light into higher orders. The approximate “flat” fill factor is only 20 to 25%. This can be seen in the graininess and relatively poor contrast of the sample images in Figure 2 and Figure 3.

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Figure 1 - 512x512 multi-level spatial light modulator.

Figure 2 - Sample images of a 512x512 FLC SLM.

Figure 3 - Sample images of a 512x512 NLC SLM.
A microscope image of some pixels on the original 512x512 SLM is shown in Figure 4. The faint white rectangles are the reflective pixel pads (one is highlighted by a black rectangle). All of the structure that can be seen within one of these rectangles is due to deformation from underlying layers of the silicon foundry process. As each layer is added, it conforms to the shape of the underlying layers. Therefore, the pixel mirrors are highly diffractive, yielding low optical efficiencies and poor contrast.

Figure 4 - Microscope image of some pixels on an original 512x512 multi-level SLM. The black rectangle highlights the region covered by one pixel pad.

A recent project performed post-foundry planarization techniques in an effort to improve the optical quality of the existing 512x512 SLMs. A new planar layer was placed on top of the existing circuitry, then new metal pixel pads were deposited on this planar layer. Figure 5 shows a small region of a planarized 512x512 SLM. Note the missing planar pixel that reveals the original rough pixel pad underneath. Light efficiency measurements have shown an approximate five fold increase in optical throughput versus the unplanarized 512x512 SLM. However, the post-foundry planarization process proved difficult and unreliable, resulting in very poor yields.

Fortunately, VLSI foundries have begun performing Chemical Mechanical Polishing (CMP) during the fabrication of silicon wafers. This is done primarily because the smaller foundry process sizes require very flat surfaces to keep the entire mask in focus. The smaller feature sizes result in larger F-number imaging systems, and hence shorter focal distances. These shorter focal distances force the silicon foundries to planarize the wafers so the entire surface can be focused for the next mask step. Two different foundries, both utilizing CMP techniques, were utilized for fabricating the two new 512x512 multi-level SLMs.
3. NEW LARGE PITCH 512X512 SLM

BNS recently developed a newer version of the 512x512 multi-level SLM with the same 15-µm pixel pitch. This device was primarily redesigned for a new foundry process in order to significantly increase light efficiency and fill factor. This new process has many advantages over the older one. It has a much smaller feature size - 0.5-µm vs. 1.2-µm, it utilizes planarization after each step of the foundry process, it has an additional metal layer, and it uses a “shiny” metal technique for the final metal layer.

The smaller feature size allows a reduction in the size of the circuits underneath each pixel pad. This results in much less distortion to each successive upper layer. The new foundry process also uses CMP planarization techniques after each layer of the foundry process has been applied. As discussed above, the CMP techniques reduce photolithography errors resulting in improved electrical yields. It has the added advantage for a spatial light modulator of yielding a very flat pixel mirror.

The original 512x512 SLM used a foundry process with only two metal layers, while this new device has three metal layers. The additional metal layer provides more options for routing signals in the chip, plus it gives better capabilities to shield the underlying silicon from photons, which can create charge carriers that effectively erase an displayed images. In the original 512 the top metal layer, M2, was used to create the pixel mirrors, and it was used to route the row lines. The row lines are used to select a specific row for addressing during data loading. Therefore, the additional metal layer, M3, gives an 80% area fill factor vs. 60% for the original 512 SLM. The M3 layer also gives greatly improved light shielding, a great benefit for applications requiring very bright illumination sources, such as projection display.

The new process also uses a “shiny” metal technique for the third and final metal layer. This shiny metal has a much higher reflectivity than normal foundry metals. Typically, silicon foundries intentionally use low reflectivity metals to reduce stray light problems during the photolithography steps due to reflections from the lower layer metals. This “shiny” metal has obvious benefits for a spatial light modulator. A microscope image of a few pixel pads is shown in Figure 6.
Figure 6 – Microscope image of a few pixels on the new large pitch 512x512 multi-level SLM chip. Compare this to the pixel pads from the original SLM shown in Figure 4. These two photographs were taken with the same microscope.

Figure 7 - Two pictures, a butterfly and the rings of Saturn, being displayed on one of the first new large pitch 512x512 multi-level SLMs filled with FLC. Notice these images contain much less noise and scatter than those shown in Figure 2 or Figure 3. The small horizontal streak on the right side is a defect that was created during the assembly process when several pixels were accidentally scratched.

This new large pitch SLM exhibits a greatly improved optical efficiency over prior BNS multi-level SLMs. Table 1 shows the relative power measured in the DC spot of the diffracted beam from the new large pitch 512 SLM, the old 512 SLM, the BNS 128x128 multi-level SLM, and a flat mirror using a 670-nm laser diode. The diode was apertured to illuminate an area less than the smallest active array size and was kept constant from one device to the next. The SLMs were measured as raw die, i.e. no liquid crystal or cover-glass was present for the measurement. Diffraction theory shows that a reflector with a pixilated surface containing an 80% area fill-factor will contain 64% of the power in the DC spot. This matches the measurement for the new large pitch 512 SLM quite well, showing the high quality of the pixel surface.
Table 1 - Relative power measurements for three generations of multi-level SLMs and a flat mirror.

<table>
<thead>
<tr>
<th>Device</th>
<th>Relative power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mirror</td>
<td>100%</td>
</tr>
<tr>
<td>New large pitch 512x512 multi-level SLM</td>
<td>65.2%</td>
</tr>
<tr>
<td>Old large pitch 512x512 multi-level SLM</td>
<td>1.0%</td>
</tr>
<tr>
<td>128x128 multi-level SLM</td>
<td>11.8%</td>
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4. NEW SMALL PITCH 512X512 SLM

BNS recently developed a new 512x512 multi-level SLM with a small pixel pitch of only 7-μm. This results in an active area of only 3.584-mm x 3.584-mm. BNS expects to receive this device from the foundry in mid-February of 2000. This device has a designed area fill factor of approximately 84%, but in reality, it will probably be slightly less depending on the details of the etch techniques. This chip will be similar to the new large pitch 512 SLM in that it uses three metal layers instead of the two metal layers found in the original 512 SLM. The foundry process used for this chip is a 0.35-μm, 2-Poly, 3-Metal process and performs planarization after each step to ensure high quality photolithography and good interconnects. Figure 6 shows a few pixels from a test chip that utilized the same pixel design and foundry process.

Figure 8 - Microscope image of a few pixels on the small pitch test chip. Each pixel has a pitch of 7.0-μm. The poor image quality is primarily due to the inability of the microscope to properly resolve these small features, and a lower light efficiency from passivation layers that will not be present in the actual SLM.

The small pitch 512 SLM was designed primarily for use in optical correlators, or other optical systems. The small pitch allows for a very compact and hence rugged optics design. The basic size of an optical correlator is driven primarily by the size of the SLMs utilized in the input and filter planes. This relationship is a function of the square of the pixel pitch as shown by Equation 1.
Equation 1 \[ f_{\text{eff}} = \frac{Nab}{\lambda} \]

where \( f_{\text{eff}} \) is the effective focal length required for the Fourier transform, \( N \) is the number of pixels, \( a \) is the pixel pitch for the first element, \( b \) is the pixel pitch for the second element, and \( \lambda \) is the wavelength of the laser source. For a typical 4-f optical correlator, the total optical path length will be approximately four focal lengths.

A 4-f correlator designed with our large pitch 512x512 multi-level SLMs, a pixel pitch of 15-µm, an off-the-shelf detector, with a 10-µm pixel pitch, and an 800-nm laser diode will result in a total optical path length of approximately 480-mm. If we instead use the small pitch SLMs with a pixel pitch of only 7-µm and the same detector and laser, the total optical path length shrinks to approximately 152-mm.

5. DRIVE ELECTRONICS

The existing prototype 512x512 drive electronics support two frames of storage at 4-bits per pixel. The SLM is refreshed at a 4-KHz frame rate but is limited to a 1-KHz new image rate. BNS is currently developing a complete new set of drive electronics with a scheduled completion in August of 2000. This new set is being designed to drive both the large pitch and the small pitch 512x512 multi-level SLM. The driver is being designed to support a refresh rate of 10-KHz and new image rate of 2.5-KHz. This new driver will also allow the user to store 8-bits per pixel instead of the current 4-bits. These 8-bits will then be mapped through a Look-Up-Table (LUT) and converted to a 10-bit signal prior to being sent to the SLM. This LUT will be used to linearize the optical response because the liquid crystal does not respond linearly to applied voltage. In addition, the on-board storage will increase from two frames to 1024 frames, and implement an external high-speed data port for fast image loading from cameras, frame grabbers, or other digital data sources. The new driver is also being designed to use either the PCI-bus, or the Compact PCI-bus. Both have nearly identical signal specifications, but the compact PCI-bus has a different connector and chassis style, more in line with the VME architecture. This new driver will also allow for the synchronization of two 512x512 SLMs and drivers for use in applications such as 4-f optical correlators or two-stage joint transform correlators.

6. ACKNOWLEDGEMENTS

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7. REFERENCES